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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,795	02/06/2002	Raul-Adrian Cernea	M-10314 US	2871
36257	7590	01/09/2004	EXAMINER	
PARSONS HSUE & DE RUNTZ LLP 655 MONTGOMERY STREET SUITE 1800 SAN FRANCISCO, CA 94111			NGUYEN, THAN VINH	
			ART UNIT	PAPER NUMBER
			2187	

DATE MAILED: 01/09/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

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**Office Action Summary**

Application No.

10/071,795

Applicant(s)

CERNEA, RAUL-ADRIAN

Examiner

Than Nguyen

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 8/1/03, 9/2/03.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) \_\_\_\_\_ is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-38 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 May 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7, 9.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

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### **DETAILED ACTION**

1. This is a response to the amendment and IDS, filed 8/1/03 and 9/2/03.
2. Claims 1-38 are pending.
3. In response to the amendment to the title, the previous objection to the title is withdrawn.
4. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection. Based on new discovered prior arts, the previous indication of allowance is withdrawn.

### ***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1-38 is rejected under 35 U.S.C. 102(b) as being anticipated by Estakhri et al (USP 5,907,856).

As to claim 1,11,29:

7. Estakhri teaches a device for storing mapping information. Estakhri teaches the claimed non-volatile memory system comprising: a controller for externally transferring data identified by logical sector addresses (controller 532; Fig. 10); and a memory connected to the controller , ((memory; 3/55-65, 4/20-24) comprising: an array comprised of a plurality of sectors, wherein

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each sector contains a plurality of data storage elements and is identified by a physical address; and a pointer structure storing correspondences between logical sector addresses and physical sector addresses, wherein the pointer structure concurrently maintains a first correspondence between a logical sector address and a first physical sector address at which currently valid data identified by the logical sector address is stored and a second correspondence between the logical sector address and a second distinct physical sector address at which previously valid data identified by the logical sector address has been stored (4/34-50, 11/64-12/20).

As to claim 2,12,33:

8. Estakhri teaches correspondences are stored in non-volatile storage elements of the pointer structure (6/22-25).

As to claim 3,14:

9. Estakhri teaches read and write circuitry coupled to the array and the pointer structure, wherein the array and the pointer structure have distinct decoder structures (flash controller 532; 10/15-17).

As to claim 4,13:

10. Estakhri teaches the correspondences are stored in binary non-volatile storage elements and the data storage elements are multi-state (12/50-13/5).

As to claim 5:

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11. Estakhri teaches the controller and said memory are formed on separate integrated circuits (Fig. 10).

As to claim 6,15,30:

12. Estakhri teaches the memory concurrently maintains the currently valid data identified by the logical sector address and the previously valid data identified by the logical sector address (11/64-12/20).

As to claim 7,19,34,35:

13. Estakhri teaches the controller can access the previously valid data identified by the logical sector address in response to a command (9/34-50; 11/64-12/20).

As to claim 8,16:

14. Estakhri teaches said memory comprising: write circuitry coupled to the memory array and the pointer structure, wherein during a write process new data corresponding to a specified logical sector address is written into the array at a new physical sector address of the array concurrently with a new correspondence between the specified logical sector address and the new physical sector address being stored in the pointer structure (11/64-12/20).

As to claim 9,17,31,32:

15. Estakhri teaches said memory further comprising: erase circuitry coupled to the array whereby said previously valid data is erasable in a background erase process (6/3-21).

As to claim 10,18:

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16. Estakhri teaches each sector of the array has an associated flag bit, the integrated circuit further comprising: a determination circuit connected to the write circuitry and the array, whereby an available sector is determined for the new physical sector address based on the associated flag bits (7/1-8/12)

As to claim 20,21,38:

17. Estakhri teaches a method of operating a memory system comprising a controller and a memory, the memory including a pointer structure and an array comprised of a plurality of sectors, wherein each sector is identified by a physical address and contains a plurality of non-volatile data storage elements, the method comprising: receiving at the controller unit from a host a first data set and a logical sector address whereby the host identifies the first data set; transferring the first data set and the logical sector address from the controller to the memory; storing the first data set at a first physical sector address of the array; storing a first correspondence between the logical sector address and the first physical sector address in the pointer structure; subsequent to said storing the first data set and said storing the first correspondence, receiving at the controller from the host a second data set to be stored at the logical sector address; transferring the second data set from the controller to the memory; storing the second data set at a second physical sector address of the array; and storing a second correspondence between the logical sector address and the second physical sector address in the pointer structure, wherein the memory retains the first data set at the first physical sector address

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and the first correspondence in the pointer structure subsequent to said storing the second data set and said storing the second correspondence (Fig 4; 7/7-8/12, 11/64-12/20).

As to claim 22:

18. Estakhri teaches storing the second data set and the second correspondence, erasing the first physical sector (6/3-21).

As to claim 23:

19. Estakhri teaches erasing is performed in a background process (6/3-21).

As to claim 24:

20. Estakhri teaches the pointer structure is non-volatile (6/22-25).

As to claim 25,26:

21. Estakhri teaches storing the second data set and the second correspondence, receiving at the controller a request from the host for data stored at the logical sector address; providing the request from the controller to the memory in terms of the logical sector address; and providing the second data set from the memory to the controller in response to the memory receiving the request in terms of the logical sector address (4/34-50, 11/64-12/20).

As to claim 27,36:

22. Estakhri teaches prior to said storing the first data set, selecting the first physical sector address from a set of available sector addresses; and prior to said storing the second data set, selecting the second physical sector address from the set of available sector addresses (7/6-8/13).

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As to claim 28,37:

23. Estakhri teaches said set of available sector addresses corresponds to only good physical sectors (good available space; 7/40-47).

*Conclusion*

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is (703) 305-3866. The examiner can normally be reached on M-F from 8:00 a.m. to 3:00 p.m. EST.

25. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

26. The fax phone number for Art Unit 2187 is 703-308-9051 or 703-308-9052.



Than Nguyen

Primary Patent Examiner

December 31, 2003